A 4-λ × 28-Gb/s/λ Silicon Ring-Resonator-Based WDM Receiver With a Reconfigurable Temperature Controller

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Abstract—We present a 4-λ × 28-Gb/s/λ silicon ring-resonator-based hybrid-integrated WDM receiver along with the reconfigurable temperature controller. Each of four ring resonators is thermally controlled so that only the target wavelength can be delivered to an integrated photodetector and processed with a hybrid-integrated CMOS TIA. The controller automatically determines the heater voltage required for each ring resonator to receive any target wavelength and maintains this condition against any external temperature fluctuations. It is experimentally verified that the controller performs its task during the initial calibration process and against the thermal stress. In addition, using the controller, WDM channel reconfiguration is successfully demonstrated.

Index Terms—Ring resonator filter, silicon photonics, temperature controller, wavelength division multiplexing (WDM), WDM receiver.

I. INTRODUCTION

THE widespread use of various services based on artificial intelligence and machine learning (AI/ML) is demanding the ever-increasing interconnect bandwidth for hardware systems in data centers [1]. Many electrical interconnects are being

replaced with optical interconnects and, Tb/s optical interconnect solutions are expected to be employed [2], [3]. Furthermore, high-performance electronic systems require photonic I/O solutions such as co-packaged optics (CPO) [4] that can provide higher bandwidth density and reduced latency, resulting in greatly enhanced overall system performance [5].

For these demanding applications, Si photonic wavelength division multiplexing (WDM) technique is the key enabler as it can deliver the required bandwidth density in a cost-effective manner [6], [7], [8], [9]. For wavelength filters required in WDM receivers, the arrayed waveguide grating (AWG) [10] and the Mach-Zehnder interferometer (MZI) [11] have been widely used. However, with these filters, it is difficult to achieve the required bandwidth density due to their relatively large size. Compared to these, ring resonator filters (RRFs) are much smaller, but their characteristics have strong dependence on the fabrication process variation as well as temperature and, consequently, an electronic controller that ensures for the RRF to have the desired filtering characteristics and maintains them against any temperature fluctuation is an absolute necessity.

The usual technique is controlling the RRF temperature using an on-chip heater. Various techniques have been used for implementing such temperature controllers (TCs) for RRFs [12], [13], [14], [15]. A simple look-up table can be used [12], but it may not be a robust solution when WDM receivers are expected to face widely changing environment. TCs based on the closed-loop feedback control of on-chip heaters with the RRF output optical power have been reported for 1-λ [13], 4-λ [14], and 8-λ [15] RRF WDM receivers. These TCs provide precise control of RRFs, but they rely on the independent closed-loop feedback for each WDM channel and, consequently, initial calibration should be done in a sequential manner for each RRF, which may involve prolonged calibration time. It can become a significant burden as the number of WDM channels grows. Therefore, a scalable calibration scheme that can minimize the calibration procedure and can be easily applied to larger channel number is an important issue in RRF temperature controller design.

In this paper, we demonstrate the centralized TC which can calibrate and maintain the entire WDM channels as a whole and, furthermore, can perform the WDM channel reconfiguration. Specifically, we present a 4-λ × 28-Gb/s/λ Si photonic WDM receiver with a TC that automatically determines the initial

on-chip heater voltage for each WDM channel with a single scanning procedure, and performs fine tuning of the heater voltages as well as maintains the optimal condition against any temperature fluctuation. And also, WDM channel reconfiguration can be performed using the found heater voltages. Since our controller can locate all WDM channels through a single scanning procedure, expanding the WDM channels is simple. The WDM receiver is realized with the hybrid integration of a Si photonic integrated circuit (PIC), which contains four silicon RRFs with on-chip heaters and Ge photodetectors (PDs), and CMOS transimpedance amplifier (TIA) electronic integrated circuit (EIC). The TC is implemented with an FPGA along with analog-to-digital converters (ADCs) for monitoring RRF transmitted optical powers and digital-to-analog converters (DACs) for driving on-chip heaters.

This paper is organized as follows. Section II provides detailed explanations for the WDM receiver structure and how the TC carries out its task. In Section III, the measurement results of the initial calibration process, the thermal stress test, and WDM channel reconfiguration are given. Finally, Section IV concludes the paper.

II. Si RRF WDM Receiver With TC

Fig. 1(a) shows the block diagram for the Si RRF-based WDM receiver and the TC. The receiver is made up of two separate chips, one PIC containing all the optical components and the other EIC containing TIAs. Two chips are connected with wire bonding on a printed circuit board (PCB), as can be seen in Fig. 1(b). In the PIC, four RRF filters share a single bus waveguide, and an integrated Ge-PD is connected to the drop port of each RRF. The PIC is fabricated with IHP's 0.25-μm Si Photonic process on a 220-nm silicon-on-insulator (SOI) substrate [16]. Each RRF has a 12-μm radius and is realized with the 500-nm wide Si rib waveguide with an N-doped silicon heater. The EIC contains four custom-designed 28-Gb/s CMOS TIA circuits fabricated with the standard 28-nm CMOS technology. The TC monitors how much the desired wavelength signal is delivered to the target Ge-PD by sampling the DC component of the photocurrent from the TIA with an ADC, and determines and delivers the required heater voltage to the corresponding RRF on-chip heater.

The red line in Fig. 2(a) shows the measured transmission characteristics of four RRFs when the light signal with varying wavelength is introduced and measured at the output of the bus waveguide without any heating of the on-chip heaters. Although all the RRFs are designed to have the identical geometry, there are slight differences in their resonance wavelengths due to the fabrication process variation and, consequently, the measured transmission peaks are broader than the resonance peak for one RRF shown in the figure for comparison. For 19 dies, the measured maximum deviation in resonance wavelength is less than 1-nm. For one RRF measurement, a single RRF having the identical geometry as the RRFs in the WDM receiver and fabricated on the same die is used. The WDM RRFs have the free spectral range (FSR) of about 8.3-nm around 1.55–1.56-μm. Fig. 2(b) shows the filter characteristics measured at the drop port

(a)

(b)
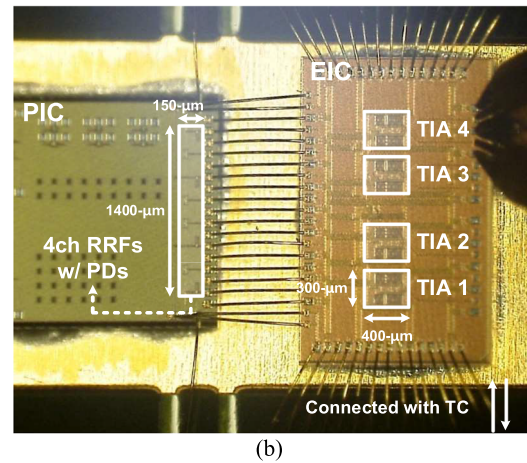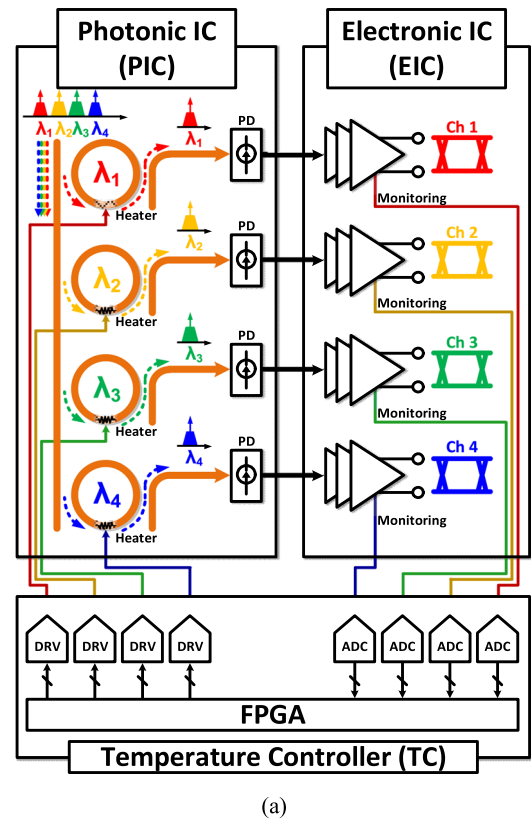
Fig. 1. (a) Block diagram for Si RRF WDM receiver and TC. (b) Chip microphotograph of WDM receiver.

of a single RRF. From this, the Q-factor is estimated to be about 2200. Fig. 2(c) shows the measured resonance wavelength shift as well as the estimated corresponding RRF temperature change with different heater powers applied. The heater is designed to have the full FSR tuning capacity within 50-mW of heater power.

Fig. 3 shows the detailed structure for a single WDM receiver. The TIA is based on inverter-based amplifiers together with inductors. The transimpedance gain with 50-Ω load is 54-dB. The TIA has a loop for DC offset cancellation (DCOC), which consists of a low-pass filter with 2.5-MHz cut-off frequency, an operational amplifier (OP-AMP), and a transistor for the DC current sink. With this DCOC loop, the received signal

Fig. 2.   (a) Measured transmission characteristics for RRF at the bus waveguide output. (b) Measured RRF drop-port characteristics. (c) Measured resonance wavelength shift with heater power for RRF.

Fig. 3.   Detailed structure and signal configuration of WDM receiver for single WDM channel.
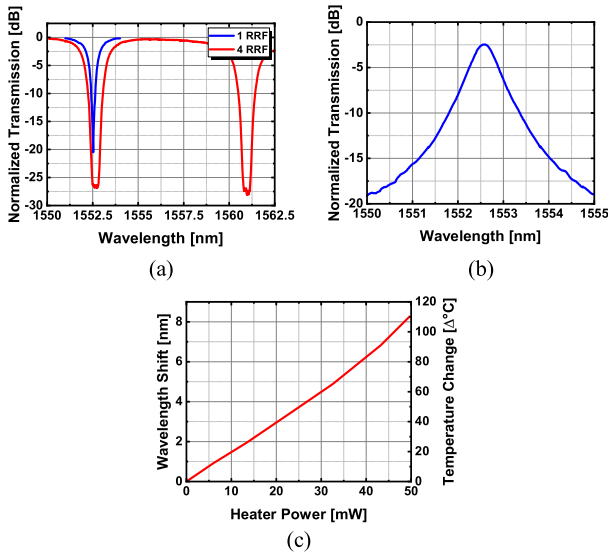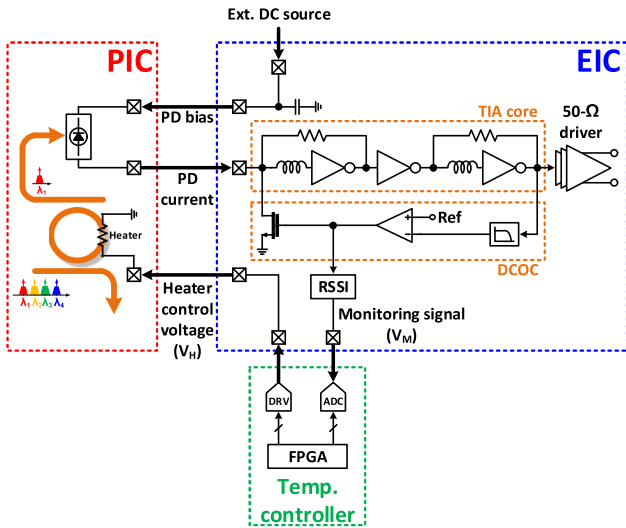

Fig. 4.   Visualization of (a) scan mode and (b) dither-and-track mode. (c) Schematic drawings for V_H and V_M during scan mode and dither-and-track mode.

strength indicator (RSSI) circuit copies the DC component of the photocurrent generated in the Ge-PD and converts it to a voltage signal (V_M). The heater control voltage (V_H) is determined in the TC and provided to the target RRF heater with the DAC-based heater driver (DRV).

The TC determines the required heater voltage for each WDM channel in two modes: scan mode and dither-and-track mode. Fig. 4(a) schematically shows the TC operation during the scan mode. It sweeps the heater control voltage for one RRF while light signals with four different wavelengths are introduced to the WDM receiver. With this scanning, four V_M peaks can be obtained for four wavelengths. Each of four V_H values that produce V_M peaks corresponds to the required V_H value for each

RRF for the resonance condition, assuming all four RRFs have identical characteristics. These V_H values are saved and applied to the corresponding RRF heaters. To find these peaks, the TC compares V_M values for the current and the previous DAC codes. The value of 1 is saved in a 1-bit register if the V_M value for the current DAC code is larger than that of the previous one, and 0 otherwise. The TC monitors the stored values and identifies the negative edge where the comparison value changes from 1 to 0 as the condition for the resonance peak for each ring resonator and stores the corresponding DAC code. Since the key of this scheme is to find the peak of the V_M, the same procedure can be applied regardless of the number of WDM channel. And since the V_H value required for each wavelength is found in this mode, those values can be utilized for WDM channel reconfiguration.

Although all the ring resonators are designed to have the same structure, their transmission characteristics may not be the same due to process variation and, consequently, V_H determined from the scanning of the first ring resonator may not be correct for other ring resonators. However, the difference is usually not too large for closely located ring resonators, and our TC correctly determine the required V_H for each ring resonator during the dither-and-track mode [17], in which the optimal V_H for each ring resonator is continuously searched by monitoring the average optical power at the drop port of each ring resonator. In the dither-and-track mode, V_H is intentionally changed slightly, and V_M values before and after the change are compared. Then, the TC determines whether V_H should be increased or decreased in order to bring the RRF resonance wavelength to the desired value. If $V_{M,after}$ is larger than $V_{M,before}$ when the TC increases or decreases V_H, the TC maintains the sign of change in V_H for the next operation same as the current operation. But if $V_{M,after}$ is smaller than $V_{M,before}$, the TC changes the sign of change in V_H for the next operation. By repeating this process, V_H and V_M values will reach a state where they dither around the values required for the desired condition, as shown in the middle of Fig. 4(b).

The amount of dithering can be made to be as small as possible so that this dithering does not influence the WDM receiver performance significantly. This dither-and-track condition can perform the required fine tuning of the heater voltages for RRFs as schematically shown in Fig. 4(c). This dither-and-track mode can be on continuously so that any influence of temperature change in the environment can be compensated. Furthermore, since the desired V_H value for each RRF is roughly determined in the scan mode and stored, the TC can use this information to reconfigure the WDM receiver channels by applying required V_H values to the reconfigured WDM receiver.

III. MEASUREMENT

To evaluate the operation of the WDM receiver and the TC, a measurement setup shown in Fig. 5 is used. The hybrid-integrated WDM receiver is mounted on a FR4 PCB which is placed on a temperature-controllable chip stage. The ADC/DRV board within the TC has four 8-bit ADCs which sample V_M values and four 8-bit DAC-based heater drivers which supply V_H up to 3-V. The FPGA logic operation is carried out with 400-Hz clock signal. The main limiting factor for the temperature control speed is the on-chip heater whose measured 3-dB thermal response bandwidth is about 8-kHz. In addition, parasitic components of commercial ADCs and drivers on the PCB result in additional feedback speed degradation when connected to the WDM receiver. If the entire TC is integrated in an IC along with the TIAs with well-optimized heater, the tracking speed can be further enhanced. The four C-band tunable laser sources (TLS) having $\lambda_1 = 1553.6$-nm, $\lambda_2 = 1555.2$-nm, $\lambda_3 = 1556.8$-nm and $\lambda_4 = 1558.4$-nm with channel spacing of 1.6nm (200-GHz) are used for the WDM input signals. For this channel spacing, our RRFs shown 13.4-dB crosstalk suppression. Further suppression can be achieved with using higher-Q RRFs. Due to the limitation in our equipment, only one WDM signal can be modulated with
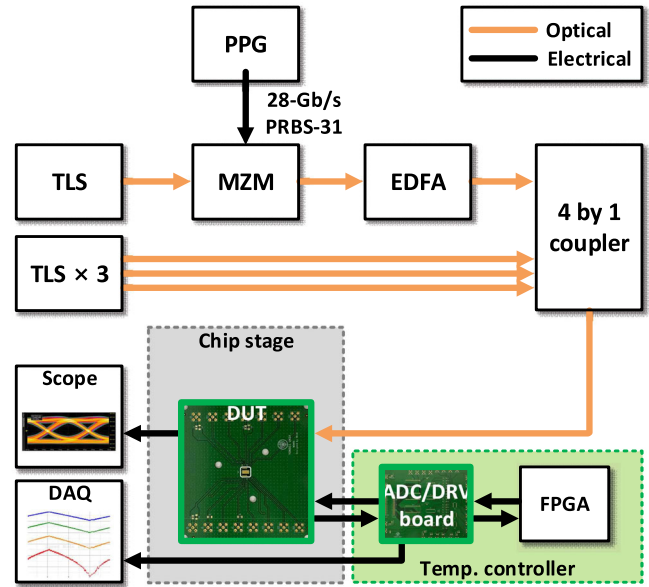

Fig. 5.　Measurement setup.
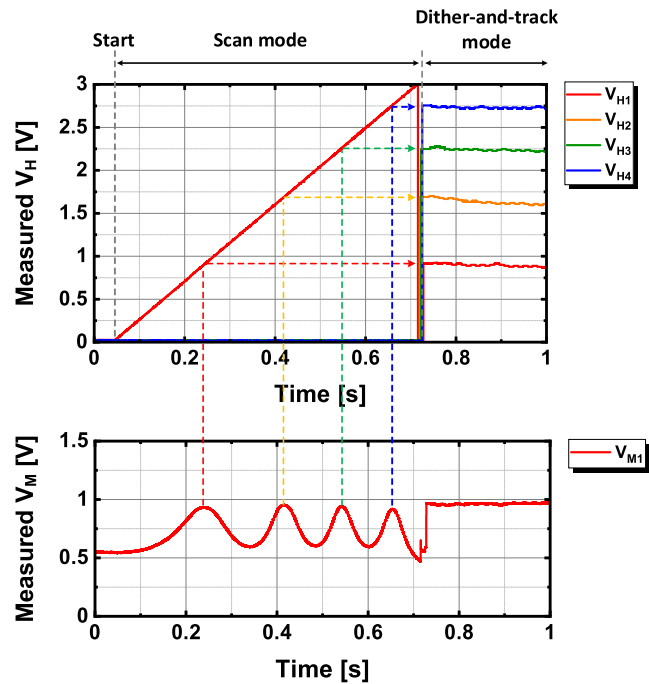
Fig. 6.　Measured V_H and V_M values with initial TC operation.

28-Gb/s, PRBS-31 data using a Mach-Zehnder modulator (MZM) at a time. The insertion loss due to this modulation is compensated with an erbium-doped fiber amplifier (EDFA). Then, four WDM signals are combined in a 4×1 coupler and are applied to the WDM receiver through a grating coupler. The output electric signals produced by the TIAs are observed with an oscilloscope. In addition, the ADC/DRV board is designed so that each of four V_M and four V_H signals can be independently monitored through data acquisition (DAQ). With this board and the built-in heater of RRF, 85% of FSR for given RRF can be

Fig. 7.   Measured BER curve and eye diagram of optical receiver for 28-Gb/s, PRBS-31 modulation data.

(a)

(a)

(b)

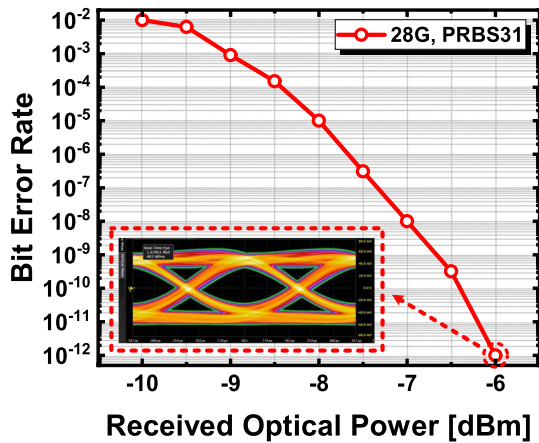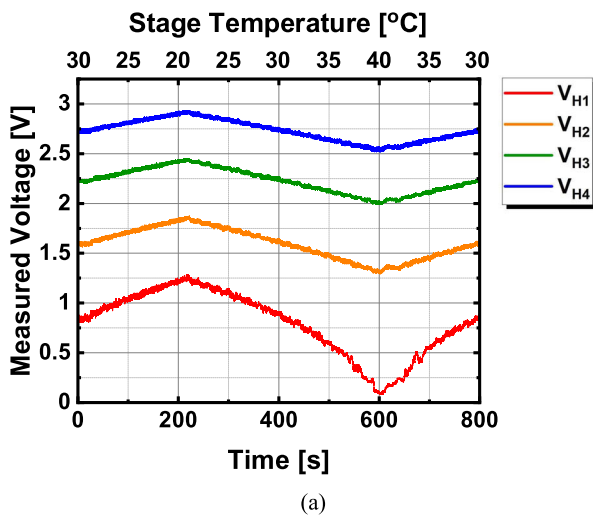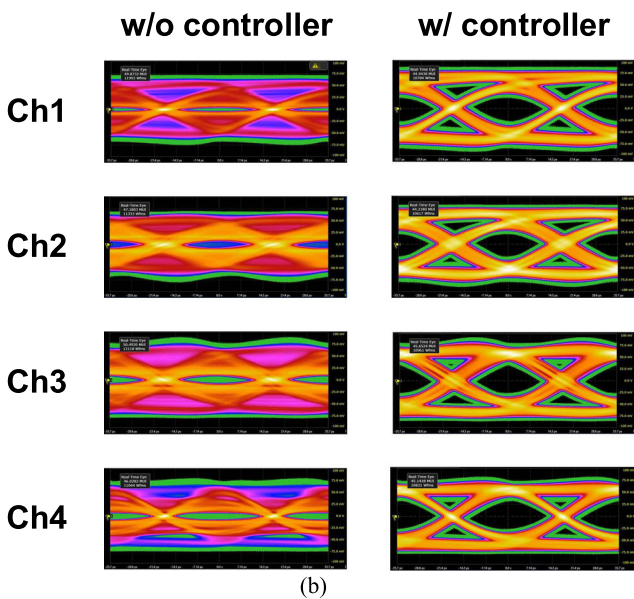Fig. 9.   (a) Channel configuration setup of WDM receiver used for reconfiguration measurement. (b) Measurement result of WDM channel reconfiguration.

tuned. Using the additional heater optimization with dedicated heater fabrication process [18] or thermal isolation techniques [19], [20], full FSR tuning becomes possible, covering all wavelength domains. Except for the thermal stress test, all the measurements are done with the chip stage temperature set at 30 °C.

Fig. 6 shows the measured V_H and V_M values during the scan mode and the dither-and-track mode. In this measurement, the first RRF in WDM filter is used in scan mode. The TC increases V_{H1} and measures V_{M1} to finds V_H values producing V_M peaks. Then, the TC assigns the desired V_H value to each RRF and carries out the dither-and-track operation.

Fig. 7 shows the measured bit error rate (BER) curve for 28-Gb/s, PRBS-31 modulation data for the varying optical power delivered to the Ge-PD for one of the WDM channels ($\lambda_4 = 1558.4$-nm) while the TC is in the dither-and-track mode. An eye diagram is also shown for -6-dBm where the BER is 10^{-12}. The dithering range of V_H is sufficient to maintain 10^{-12} of BER. For this measurement, -6-dBm DC WDM signals are delivered to Ge-PDs of other WDM channels. Each TIA consumes 27-mW with 1.2-V supply voltage.
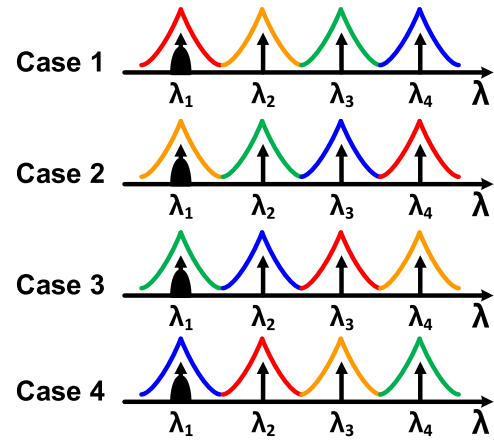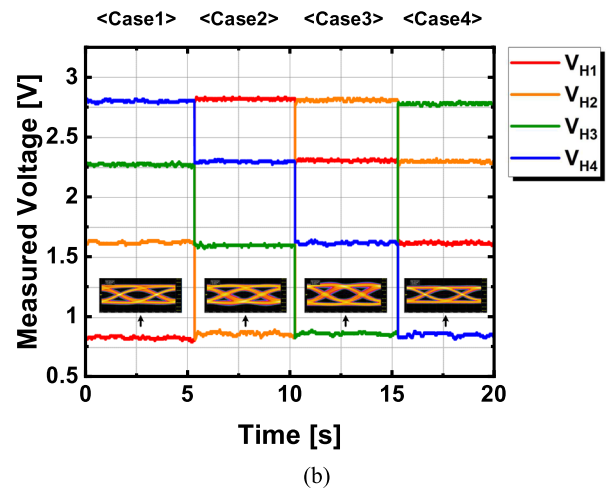

(b)

Fig. 8.   (a) Measurement result of V_H values when chip stage temperature changes. (b) 28-Gb/s accumulated eye diagram of each channel for 800 seconds without and with TC operation.

Fig. 8(a) shows the measured V_H values during the thermal stress. For the thermal stress, the chip stage temperature is reduced from 30 °C to 20 °C, then increased to 40 °C, and then reduced back to 30 °C with the temperature change rate of 0.05 °C/s. Faster temperature change was not possible since the temperature of the entire stage was changed for this measurement. With this thermal stress, V_H values should go up initially, then go down, and then up for all RRFs as can be seen from the measured V_H values shown in the F. The V_H value is higher for the higher WDM channel because its RRF has the larger resonance wavelength requiring higher temperature. In addition, the amount of change in V_H in response to the thermal stress is smaller for the higher WDM channel because heating power is proportional to V_H^2 and, consequently, smaller change in V_H can produce the required temperature change.

Fig. 8(b) shows accumulated eye diagrams for each WDM channel during 800 seconds of above thermal stress without and with TC operation. For each of these measurements, the selected WDM channel is modulated with 28-Gb/s, PRBS-31 data for -6-dBm received optical power while other three WDM channels are supplied with -6-dBm DC power. The measured accumulated BER is 3.9×10^{-10} for WDM channel 4. The BER degradation is believed due to the Q-factor RRF change at different temperatures.

Since the TC determines the approximate V_H value for each input wavelength during the scan mode, this information can be used for WDM channel reconfiguration. To verify this, the WDM channel configuration is changed during the dither-and-track mode for four different cases shown in Fig. 9(a) and measured V_H values are shown in Fig. 9(b). Also shown are the measured 28-Gb/s PRBS-31 eye diagrams for channel No.1 ($\lambda_1 = 1553.6$-nm). For the eye diagram measurement, measurement during the transition period was avoided. Clearly, these results demonstrate the WDM channel reconfiguration capacity of our TC.

IV. CONCLUSION

We present a Si ring-resonator based WDM receiver with the reconfigurable temperature controller. The WDM receiver is realized with a PIC consisting of 4-channel ring-resonator based WDM filters and Ge-PDs hybrid-bonded with an EIC containing four custom-designed TIAs fabricated with a 28-nm CMOS process. The temperature controller initially scans and determines the required RRF on-chip heater driving voltages, and fine-tune the driving voltages and maintain the optimal condition against any temperature using the simple dither-and-track operation. In addition, the TC is capable of reconfiguring WDM channels without any additional hardware or TC modification. Since the operation of our TC is based on simple control algorithm, it is scalable and can be easily implemented with an IC, which should be of great advantage for Si photonic WDM receivers for photonic I/O solutions.

ACKNOWLEDGMENT

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